

### Technical Data

### S1300 / S1309 / ST1300 / ST1309 Series



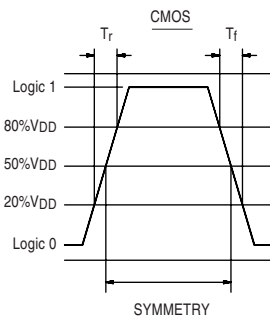
#### Description

A 3.3V, voltage controlled crystal oscillator with output logic levels compatible with LVCMOS and LVTTTL logic families. The series is designed with excellent Jitter characteristics which makes it ideal for use in Telecom and Datacom applications. True SMD DIL versions for IR reflow are available, select option "S" in part number builder. See separate data sheet for SMD package dimensions.

#### Applications & Features

- Phase-Locked Loop (PLL) Clock and Data Recovery, Frequency Transaltion, Frequency Synthesis apps in Video, Video Compression, Telephony, and LAN/WAN Data Communication
- 3.3 Volt operations
- LVCMOS / LVTTTL compatible
- 3.5ps max RMS period jitter
- Wide range of performance options:
  - ±50 to ±100 ppm APR\*
  - ±20 to ±50 ppm Frequency Stability
- Tri-State option
- True SMD for IR reflow available

#### Output Waveform



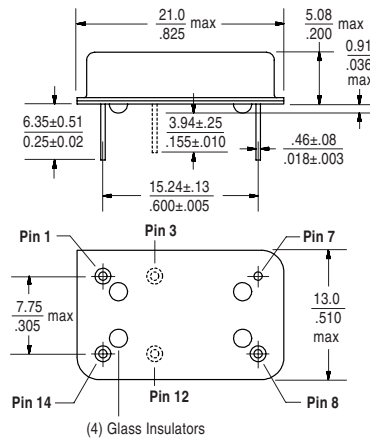
<b>Frequency Range:</b>	1.5 MHz to 28.6363 MHz
<b>Frequency Stability:</b>	±20, ±25 or ±50ppm over all conditions: operating temperature, voltage change, load change, calibration tolerance, shock and vibration, with $V_C = 1.65V$
<b>Aging @ 25°C:</b>	± 3ppm max per year, ±10ppm max for 10 years
<b>Temperature Range:</b>	Operating: 0 to +70°C or -40 to +85°C Storage: -55 to +125°C
<b>Supply Voltage:</b>	Recommended Operating: 3.3V ±10%
<b>Supply Current:</b>	10mA typ, 15mA max
<b>Output Drive:</b>	Symmetry: 45/55% max @ 50% VDD Rise & Fall Times: 9ns max 20% to 80% VDD Logic 0: 10% VDD max Logic 1: 90% VDD min Load: 30pF Jitter: 3.5ps max RMS period jitter
<b>Pull Characteristics:</b>	Input Impedance (pin 1): 50KΩ min Frequency Response (-3dB): 10 kHz min Pullability: ±50, ±70, ±100ppm APR* min Control Voltage: 0.3 to 3.0V Transfer Function: Frequency Increases when Control Voltage Increases Linearity: 5 or 10% max Center Control Voltage: 1.65V
<b>Mechanical:</b>	Shock: MIL-STD-883, Method 2002, Condition B Solderability: MIL-STD-883, Method 2003 Terminal Strength: MIL-STD-883, Method 2004, Condition B2 Vibration: MIL-STD-883, Method 2007, Condition A Solvent Resistance: MIL-STD-202, Method 215 Resistance to Soldering Heat: MIL-STD-202, Method 210, Conditions A, B or C (I or J for Gull Wing)
<b>Environmental:</b>	Gross Leak Test: MIL-STD-883C, Method 1014, Condition C Fine Leak Test: MIL-STD-883C, Method 1014, Condition A2 Thermal Shock: MIL-STD-883C, Method 1011, Condition A Moisture Resistance: MIL-STD-883C, Method 1004

\* APR = (VCXO Pull relative to specified Output Frequency) – (VCXO Frequency Stability)  
NOTE: APR is inclusive of 10 Years Aging

### Technical Data

### S1300 / S1309 / ST1300 / ST1309 Series

#### Package Details

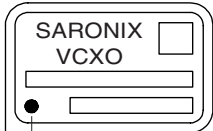


#### Pin Function:

- Pin 1: Control Voltage
- Pin 3: Tri-State control (optional)
- Pin 7: GND/Case (VSS)
- Pin 8: OUTPUT
- Pin 12: N/C (optional)
- Pin 14: +3.3VDC (VDD)

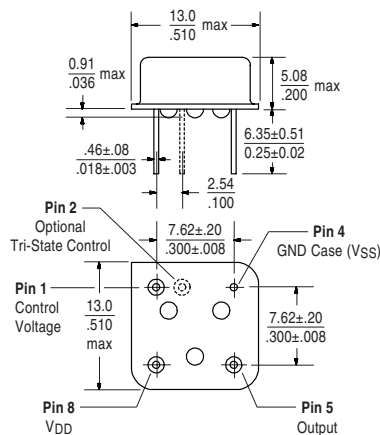
#### Marking Format\*\*

Includes Date Code, Frequency & Part Number



Denotes Pin 1

#### HALF SIZE PACKAGE



#### Marking Format\*\*

Includes Date Code, Frequency & Part Number

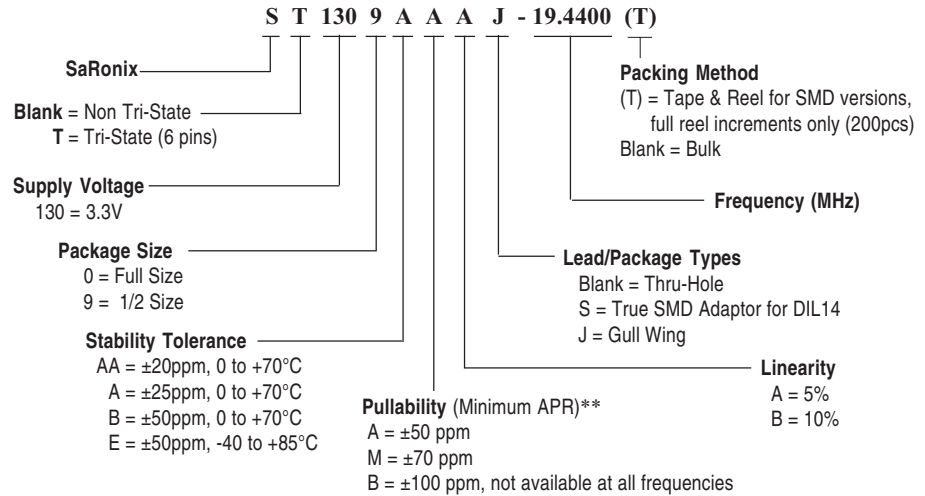


Denotes Pin 1

\*\*Exact location of items may vary

Scale: None (Dimensions in  $\frac{\text{mm}}{\text{inches}}$ )

#### Part Numbering Guide



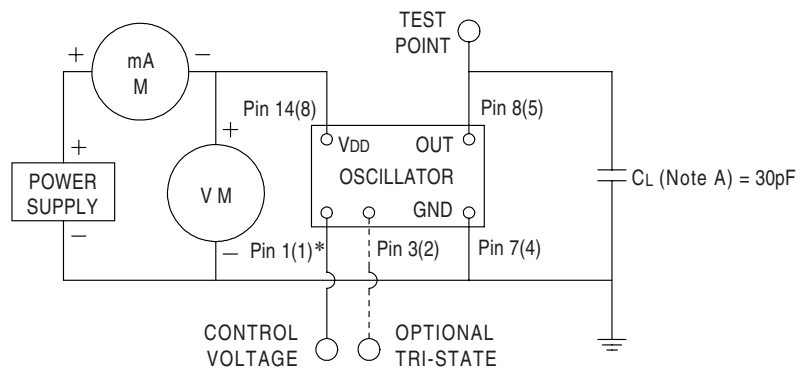
\*\* APR = (VCXO Pull relative to specified Output Frequency) - (VCXO Frequency Stability)  
NOTE: APR is inclusive of 10 Years Aging

#### Tri-State Logic Table

Pin 3(2) Input	Pin 8(5) Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 3(2):  
Logic 1 = 0.7 V<sub>DD</sub> min  
Logic 0 = 0.3 V<sub>DD</sub> max

#### Test Circuit



NOTE A: C<sub>L</sub> includes probe and fixture capacitance

\* Items in brackets ( ) represent Half Size model

All specifications are subject to change without notice.

DS-126 REV E

## True SMD Adaptor

### Technical Data

